## Notice of References Cited Application/Control No. | Applicant(s)/Patent Under | Reexamination | LU, ZIYANG | Examiner | Art Unit | Page 1 of 1

## U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
F	Α	US-6,715,093	03-2004	Farmer et al.	713/400
4	В	US-2004/0158760 a1	08-2004	Farmer et al.	713/500
7	С	US-6,557,128	04-2003	Turnquist, James Alan	714/724
7	D	US-6,651,205	11-2003	Takahashi, Koji	714/738
R	Ε	US-6,678,643	01-2004	Turnquist et al.	703/14
4	F	US-2002/0184560 a1	12-2002	Wang et al.	714/25
*	G	US-5,867,695	02-1999	Amini et al.	713/503
1/2	Н	US-6,557,133	04-2003	Gomes, Glen A.	714/738
	ı	US-			
	J	US-			
	К	US-			
	,L	US-			
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Q					
	R					
	s					
	Т					

## **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	υ	Sehgal et al., "SOC Test Planning Using Virtual Test Access Architectures", IEEE, 2004.
	V	Schmid et al., "Advanced Synchronous Scan Test Methodology for Multi Clock Domain ASICs", IEEE, unknown date.
	w	Ashkinazy et al., "Tools for Validating Asynchronous Digital Circuits", IEEE, 1994.
	x	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.